IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Huy T. Vo

Title: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR MEMORY DEVICES

Docket No.: 303.723US1
Filed: March 15, 2001
Examiner: Son Luu Mai

Serial No.: 09/808,750
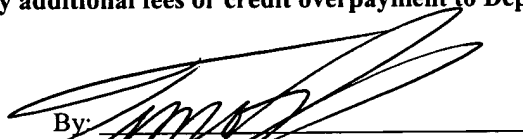Due Date: March 30, 2006
Group Art Unit: 2827

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

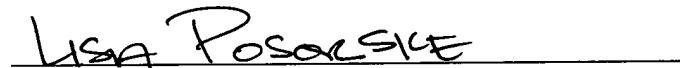We are transmitting herewith the following attached items (as indicated with an "X"):

X   Return postcard.
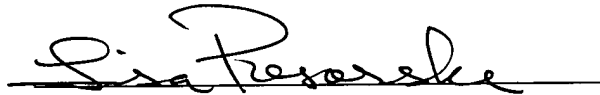X   Response Under 37 CFR 1.116 (19 pgs.).

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: _____
Atty: Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30 day of March, 2006.

Lisa Rosorsky
Name

_____
Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Huy T. Vo   Examiner: Son Luu Mai

Serial No.: 09/659,664   Group Art Unit: 2827

Filed: March 15, 2001   Docket: 303.723US1

For: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN
SEMICONDUCTOR MEMORY DEVICES

RESPONSE UNDER 37 C.F.R. § 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This responds to the Final Office Action dated January 30, 2006.

RESPONSE UNDER 37 C.F.R. § 1.116
Serial Number: 09/808,750
Filing Date: March 15, 2001
Title: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR DEVICES

Page 2
Dkt: 303.723US1

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the Assignee, Micron Technology, Inc.

RESPONSE UNDER 37 C.F.R. § 1.116
Serial Number: 09/808,750
Filing Date: March 15, 2001
Title: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR DEVICES

Page 3
Dkt: 303.723US1

2. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Applicant.

RESPONSE UNDER 37 C.F.R. § 1.116
Serial Number: 09/808,750
Filing Date: March 15, 2001
Title: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR DEVICES

Page 3
Dkt: 303.723US1

3. STATUS OF THE CLAIMS

The present application was filed on March 15, 2001 with claims 1-54. In the first Office Action, claims 1-54 were rejected. In a response to this Office Action filed August 21, 2002, claims 1, 8, 15, 19, 26, 30, 37, 42, 45, and 49 were amended. No claims were canceled. A first Final Office Action (which was the second office action) was mailed October 18, 2002 that rejected claims 1-54. A response to the first Final Office Action filed December 18, 2002 did not amend or cancel any claims. An Advisory Action mailed January 24, 2003 indicated that the application was not in condition for allowance. A Request for Continued Examination was filed February 19, 2003 along with amendments to claims 1, 5, 8, 15, 19, 26, 30, 37, 42, 45, and 49. No claims were canceled.

A third Office Action was mailed March 7, 2003 rejecting claims 1-54. A response to the third Office Action mailed June 9, 2003 did not amend or cancel any claims. A second Final Office Action (which was the fourth office action) was mailed June 25, 2003 that rejected claims 1-54. In a response to the second Final Office Action filed August 25, 2003, claims 1, 5, 8, 15, 19, 26, 30, 37, 42, 45, and 49 were amended. No claims were canceled. An Advisory Action was mailed October 6, 2003 that indicated the application was not in condition for allowance because the amendments raise new issues that would require further consideration and/or searching. A Request for Continued Examination was filed October 15, 2003 to have the Examiner consider the amendments.

A fifth Office Action was mailed December 10, 2003 rejecting claims 1-54. A response to the fifth Office Action was filed March 10, 2004 that amended claims 1, 5, 8, 15, 19, 26, 30, 37, 45, and 49. Claims 42-44 were canceled. Claims 1-41 and 45-54 were pending in the application. A third Final Office Action was mailed May 21, 2004 that rejected claims 1-41 and 45-54. In a response to the third Final Office Action filed July 21, 2004, claims 1, 5, 8, 15, 19, 26, 30, 37, 45, and 49 were amended. No claims were canceled. An Advisory Action was mailed August 12, 2004 that indicated the application

was not in condition for allowance because the amendments raised new issues that required further consideration and/or searching. A Request for Continued Examination was filed August 23, 2004 to have the Examiner consider the amendments.

A seventh Office Action was mailed October 19, 2004 rejecting claims 1-41, 45-54. A response to the seventh Office Action was filed March 10, 2004 that amended claims 1, 5, 8, 15, 19, 26, 30, 37, 45, and 49. No claims were canceled. A fourth Final Office Action was mailed April 15, 2006 that rejected claims 1-41 and 45-54. In a response to the fourth Final Office Action filed June 15, 2005, claims 1, 5, 8, 15, 19, 26, 30, 37, 45, and 49 were amended. No claims were canceled. An Advisory Action was mailed July 5, 2005 that indicated the application was not in condition for allowance because the amendments raised new issues that required further consideration and/or searching. A Request for Continued Examination was filed July 12, 2005 to have the Examiner consider the amendments.

A ninth Office Action was mailed August 26, 2005 rejecting claims 1-41, 45-54. A response to the seventh Office Action was filed November 28, 2005 that amended claims 1, 5, 8, 15, 19, 26, 30, 37, 45, and 49. No claims were canceled. A Supplemental Amendment was filed December 5, 2006 adding claims 55-57. Claims 1-41, 45-57 were pending in the application. A fifth Final Office Action was mailed January 30, 2006 that rejected claims 1-41 and 45-57.

Thus, claims 1-41, 45-57 stand rejected and remain pending.

RESPONSE UNDER 37 C.F.R. § 1.116
Serial Number: 09/808,750
Filing Date: March 15, 2001
Title: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR DEVICES

Page 6
Dkt: 303.723US1

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Office Action which was mailed January 30, 2006.

5. SUMMARY OF CLAIMED SUBJECT MATTER

As noted in the background section of the present patent application, the performance of a dynamic random access memory (DRAM) is largely dependent on the resistance of the DRAM circuitry. A lower resistance in the circuit leads to a lower value of a resistance-capacitance (RC) time constant, and a faster performing memory device. The RC time constant is especially affected by wordline design due to the extended length of word lines, and their necessarily small size as they are integrated into access transistors. In ultra large scale integrated (ULSI) circuits, a highly conductive word line is necessary to improve circuit density and performance. It therefore follows, that the problem of wordline RC losses must be overcome. As devices are scaled down in size, word line widths are also decreased. Both the smaller cross section of wordlines, and the increased length of wordlines in ULSI circuits contribute to increased resistance (pg. 1 line 18 to pg. 2 line 7).

Wordlines are frequently made of polysilicon, however polysilicon has a relatively high resistivity compared to other metal materials. One approach to lowering wordline resistivity has been to add a second layer of lower resistivity metal on top of a polysilicon wordline to make a two layer wordline. The aim of this approach is to lower the resistivity of the entire wordline, and as a result to accommodate the large number of memory cells that a wordline must access in a ULSI circuit. A significant problem with this approach has been the compatibility of the polysilicon with the second metal layer. They tend to diffuse into each other, and the low resistivity of the metal layer is drastically compromised (pg. 2 lines 10–17).

The present application describes memory arrays, memory devices, integrated circuits, information handling devices, methods of reducing a wordline RC time constant, and methods of forming a memory device. A memory array taught by Applicant and claimed in claims 1-4 includes a strapping line of lower resistance than the wordlines coupled to a single continuous wordline in a single array. The strapping line bypasses only a portion in a middle region between a first and second end of the single continuous

wordline, and bypasses only a portion of a wordline within the single memory array. The memory array also includes at least two channels connecting the strapping line to a first and second end of the portion of the single continuous wordline (FIG. 5 and pg. 6 line 20 to pg. 7 line 10). An integrated circuit having such a memory array is claimed in claims 15-18. An information handling device having such a memory array is taught and claimed in claims 26-29 (pg. 5 lines 8-9, pg. 6 lines 14-16, pg. 6 line 20 to pg. 7 line 10).

A memory array having a plurality of separate strapping lines and a plurality of channels connecting the plurality of strapping lines is taught by the Applicant and claimed in claims 5-7. An integrated circuit having such a memory array is claimed in claims 19-25. An information handling device having such a memory array is taught and claimed in claims 30-36 (pg. 5 lines 8-9, pg. 6 lines 14-16, pg. 6 line 20 to pg. 7 line 10).

A memory device having a number of strapping devices is taught by Applicant and claimed in claims 8-14 (pg. 5 lines 8-16 and line 24, and pg. 6 line 20 to pg. 7 line 10). A memory device taught by Applicant and claimed in claims 55-57 includes a number of parallel wordlines local to a memory array coupled to gate regions of memory cells. The even wordlines are coupled to the even row decoder and one or more odd wordlines are coupled to the odd row decoder. The odd wordlines are arranged alternately with the even wordlines. The memory device also includes a number of strapping lines having lower resistance than the wordlines which are connected to bypass portions of the wordlines within the memory array. A strapping line is connected to an odd wordline so that it bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, and a strapping line is connected to an even wordline so that it bypasses only a portion of the even wordline within the memory array nearer the even row decoder (FIG. 5, pg. 6 lines 4-7, pg. 6 line 20 to pg. 7 line 10, and pg. 8 lines 14-22).

A method of reducing a wordline RC time constant is taught by Applicant and claimed in claims 37-41. The method includes spacing a number of strapping devices over wordlines within a single memory array apart from adjacent strapping devices by a distance greater than a wordline pitch. The strapping devices bypass different portions of adjacent wordlines within the single memory array. A signal is used to bypass a first

portion of the wordline through a strapping device of lower resistance than the first portion of the wordline (FIG. 5, pg. 6 line 20 to pg. 7 line 27).

A method of forming a memory device is taught by Applicant and claimed in claims 45-48. The method includes attaching a strapping line of lower resistance than the wordlines to a single continuous wordline that bypasses only a portion in a middle region between a first and second end of the single continuous wordline. The strapping line bypasses only a portion of a wordline within the memory cell array and bypasses a different portion of a wordline within the memory cell array than an adjacent strapping line (FIG. 5, pg. 6 line 20 to pg. 7 line 10). A method of forming a memory device that includes attaching a number of strapping lines is claimed in claims 49-54.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Applicants refer to the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Are claims 1-41 and 45-57 properly rejected under 35 U.S.C. § 102(b) for anticipation by Cowles (U.S. 5,940,315)?

7. ARGUMENT

Rejections under 35 U.S.C. § 102(b).

1) Applicable Law

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. M.P.E.P § 2131. To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. V. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e. identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Applicant respectfully submits that the Final Office Action mailed January 30, 2006 (hereinafter "the Final Office Action") did not make out a *prima facie* case of anticipation because Cowles does not teach each and every claim element arranged as in the claims.

A claim in dependent form shall be construed to incorporate by reference all of the limitations of the claim to which it refers. 35 U.S.C. § 112 ¶4. Thus, if a reference does not anticipate a base claim, the reference does not anticipate a claim that depends on the base claim.

2) Discussion of the rejection of claims 1-41 and 45-57 under 35 U.S.C. § 102(b) as anticipated by Cowles(U.S. Pat. No. 5,940,315)

Claims 1-41 and 45-57 were rejected under 35 USC § 102(b) as being anticipated by Cowles (U.S. Patent No. 5,940,315, hereinafter "Cowles"). This rejection is respectfully traversed. Applicant respectfully submits that the Final Office Action has not made an improper *prima facie* showing of anticipation at least because Cowles fails to teach each and every element of claims 1-41 and 45-57.

a. Discussion of the rejection of claims 1-4, 8-14, 15-18, and 26-29

The Final Office Action admits that Cowles does not show "a number of memory cells," a number of source lines," or "a number of bit lines" (see Final Office Action page 2 ¶4). As such, the Final Office Action has not made a *prima facie* case of anticipation. The Final Office Action asserts that the missing elements are inherent in Cowles' teachings, and that by reading any reference cited in the References Cited section of Cowles, one would find all these limitations (see Final Office Action pages 6 and 7). Applicant respectfully submits that the Final Office Action has not established a *prima facie* case of inherency because, as stated in M.P.E.P. § 2131.01, to serve as an anticipation when a reference is silent about the asserted inherent characteristic, the gap in the reference may be filled with recourse to extrinsic evidence. But, such evidence must make clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.,* 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). Applicant respectfully submits that the Examiner has not produced proper extrinsic evidence to show that the elements "a number of memory cells," a number of source lines," and "a number of bit lines" recited in claim 1, 8, 15, and 26 are necessarily present in Cowles.

i.) Discussion of claims 1-4

Applicant cannot find in Cowles, among other things,

> a strapping line of lower resistance than the wordlines coupled to a single continuous wordline in a single array wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch, and wherein the strapping line bypasses only a portion of a wordline within the single array and bypasses a different portion of a wordline within the single array than an adjacent strapping line,

as recited in claim 1 or incorporated in claims 2-4. The conductive straps of Cowles bypass a wordline across an entire memory array (see e.g., FIG. 2A of Cowles), instead of only a portion of a wordline within the single array as recited in claim 1. The Final

Office Action asserts that the memory bank 100 of Cowles reads on the single memory

array recited in claim 1 (*see* Final Office Action pg. 3), and apparently asserts that

because Cowles shows metal straps spanning wordlines of the memory arrays within the

memory bank Cowles therefore bypasses a different portion of a wordline within the

memory array.

However, the memory bank 100 of Cowles is made of more than one memory

array (*see* FIG. 2A), and Cowles states that the invention ... may be used with any

number of arrays greater than one (*see* col. 3 lines 23-27). Cowles also states that

"[s]traps 112, 113 are connected to wordlines 31, 33 respectively outside the edge of

[memory] array 21 as shown in FIG. 2A at nodes 150, 151 through a contact hole in the

poly layers (see Cowles, col. 4 lines 2-4). Thus, Cowles does not disclose the structure

recited in claim 1.

ii.) Discussion of claims 8-14

Applicant cannot find in Cowles, among other things,

> a number of strapping devices which bypass portions of the wordlines in
> the single array of parallel wordlines, wherein at least one portion of a
> single continuous wordline is only in a middle region between a first and
> second end of the single continuous wordline, and wherein adjacent
> strapping devices bypass only a portion of a wordline within the memory
> array and bypass different portions of adjacent wordlines within the
> memory array,

as recited in claim 8 or incorporated in claims 9-14.

iii.) Discussion of claims 15-18

Applicant cannot find in Cowles, among other things,

> a strapping line of lower resistance than the wordlines coupled to a single
> continuous wordline wherein the strapping line bypasses only a portion of
> the wordline within the memory array in a middle region between a first
> and second end of the single continuous wordline, wherein the strapping
> line is spaced apart from adjacent conductive structures by a distance
> greater than a wordline pitch, and wherein the strapping line bypasses a
> different portion of a wordline within the memory array than an adjacent
> strapping line,

as recited in claim 15 or incorporated in claims 16-18.

iv.) Discussion of claims 26-29

Applicant cannot find in Cowles, among other things,

a strapping line of lower resistance than the wordlines coupled to a single
continuous wordline wherein the strapping line bypasses only a portion in
a middle region between a first and second end of the single continuous
wordline and bypasses only a portion of the wordline within the memory
array, wherein the strapping line is spaced apart from adjacent conductive
structures by a distance greater than a wordline pitch, and wherein the
strapping line bypasses a different portion of a wordline within the
memory array than an adjacent strapping line,

as recited in claim 26 or incorporated in claims 27-29.

Applicant respectfully requests reconsideration and allowance of claims 1-
4, 8-14, 15-18, and 26-29.

b. Discussion of the rejection of claims 5-7, 19-25, 30-36, 37-41, 45-48, and 49-54

i) Discussion of claims 5-7

Applicant cannot find in Cowles, among other things,

a plurality of separate strapping lines of lower resistance than the
wordlines coupled to at least one of the number of wordlines in a single
array wherein the strapping lines bypass a plurality of separate portions of
a single continuous wordline, and wherein adjacent strapping lines bypass
only a portion of a wordline within the memory array and bypass different
portions of adjacent wordlines within the memory array,

as recited in claim 5 or incorporated in claims 6-7. The conductive straps of Cowles

apparently bypass a wordline across an entire memory array (see e.g., FIG. 2A), instead

of only a portion of a wordline within the memory array as recited in claim 5. The

memory bank 100 of Cowles is made of more than one memory array (see FIG. 2A), and

Cowles states that the invention ... may be used with any number of arrays greater than

one (see col. 3 lines 23-27). Cowles also states that "[s]traps 112, 113 are connected to

wordlines 31, 33 respectively outside the edge of [memory] array 21 as shown in FIG. 2A

at nodes 150, 151 through a contact hole in the poly layers (see Cowles, col. 4 lines 2-4).

Thus, Cowles does not disclose the structure recited in claim 5. For example, Cowles

does not contain any disclosure of "wherein adjacent strapping lines bypass only a portion of a wordline within the memory array", or any disclosure of "[wherein adjacent strapping lines] bypass different portions of adjacent wordlines within the memory array," as recited in claim 5.

ii) Discussion of claims 19-25

Applicant cannot find in Cowles, among other things,

> a number of separate strapping devices which bypass separate portions of a single continuous wordline in the single array of parallel wordlines, and wherein adjacent strapping devices bypass only a portion of a wordline within the memory array and bypass different portions of adjacent wordlines within the single array,

as recited in claim 19 or incorporated in claims 20-25.

iii) Discussion of claims 30-36

Applicant cannot find in Cowles, among other things,

> a number of strapping devices which bypass only portions of the wordlines in the single array of parallel wordlines, wherein at least one portion of a single continuous wordline is in a middle region between a first and second end of the single continuous wordline, and wherein adjacent strapping devices bypass only a portion of the wordline within the memory array and bypass different portions of adjacent wordlines within the memory array,

as recited in claim 30 or incorporated in claims 31-36.

iv) Discussion of claims 37-41

Applicant cannot find in Cowles, among other things,

> spacing a number of strapping devices over wordlines within a single memory array apart from adjacent strapping devices by a distance greater than a wordline pitch, wherein adjacent strapping devices bypass different portions of adjacent wordlines within the single memory array,

as recited in claim 37 or incorporated in claims 38-41.

v) Discussion of claims 45-48

Applicant cannot find in Cowles, among other things,

> attaching a strapping line of lower resistance than the wordlines to a single continuous wordline wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous

wordline, wherein the strapping line is spaced apart from adjacent conductive structures by a spacing greater than a wordline pitch and wherein the strapping line bypasses only a portion of a wordline within the memory cell array and bypasses a different portion of a wordline within the memory cell array than an adjacent strapping line,

as recited in claim 45 or incorporated in claims 46-48.

vi) Discussion of claims 49-54

Applicant cannot find in Cowles, among other things,

attaching a number of strapping lines of lower resistance than the wordlines which bypass portions of the wordlines in the array of parallel wordlines, wherein at least one portion of a single continuous wordline is only in a middle region between a first and second end of the single continuous wordline, wherein the strapping lines are each located a distance from each other that is greater than the pitch, and wherein adjacent strapping lines bypass different portions of adjacent wordlines within the single array,

as recited in claim 49 or incorporated in claims 50-54.

Applicant respectfully requests reconsideration and allowance of claims 5-7, 19-25, 30-36, 37-41, 45-48, and 49-54.

c. Discussion of the rejection of claims 55-57

Applicant cannot find in Cowles, among other things,

a number of strapping lines having lower resistance than the wordlines and connected to bypass portions of the wordlines within the memory array, wherein a strapping line connected to an odd wordline bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, wherein a strapping line connected to an even wordline bypasses only a portion of the even wordline within the memory array nearer the even row decoder,

as recited in claim 55 or incorporated in claims 56-57.

The conductive straps of Cowles apparently bypass a wordline across an entire memory array (see e.g., FIG. 2A), instead of only a portion of a wordline within the memory array as recited in claim 5. The memory bank 100 of Cowles is made of more than one memory array (see FIG. 2A), and Cowles states that the invention ... may be

used with any number of arrays greater than one (*see* col. 3 lines 23-27). Cowles also

states that "[s]traps 112, 113 are connected to wordlines 31, 33 respectively outside the

edge of [memory] array 21 as shown in FIG. 2A at nodes 150, 151 through a contact hole

in the poly layers (see Cowles, col. 4 lines 2-4). Thus, Cowles does not disclose the

structure recited in claim 55.

Claim 55 also recites

> an even row decoder located on a first side of the memory array, an odd
> row decoder located on a second side of the memory array, ... wherein a
> strapping line connected to an odd wordline bypasses only a portion of the
> odd wordline within the memory array nearer the odd row decoder,
> wherein a strapping line connected to an even wordline bypasses only a
> portion of the even wordline within the memory array nearer the even row
> decoder.

Cowles describes,

> "[r]ow decoders 50 and 54 are designated as even row decoders, and row
> decoder 52 is designated as an odd row decoder. Row decoder 50 is
> positioned adjacent to memory array 20 on the opposite side of memory
> array 21, row decoder 52 is positioned between memory array 21 and
> memory array 22 and row decoder 54 is positioned adjacent to memory
> array 23 on the opposite side of memory array 22 as shown"

(see Cowles, FIG. 2A and col. 3 lines 39-46). Thus, Cowles refers to an arrangement

where an even row decoder is on one side of two memory arrays and an odd row decoder

is on an opposite side of the two memory arrays, and therefore Cowles does not describe

the structure recited in claim 55.

Applicant respectfully requests reconsideration and allowance of claims 55-57.

d. Conclusion

Applicant respectfully submits that the *prima facie* case of anticipation is improper because each and every element as set forth in the claims is not found, either expressly or inherently described, in Cowles. Therefore, Applicant requests reversal of the 35 U.S.C. § 102(b) rejection and allowance of claims 1-41 and 45-57.

8. SUMMARY

It is respectfully submitted that a *prima facie* case of anticipation under 35 U.S.C. § 102(b) has not been established. Therefore, it is respectfully requested that the rejection of Claims 1-41 and 45-57 be overturned. Applicant further submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to contact Applicant's Attorney, Timothy B.Clise, at (612) 349-9587, if prosecution will be assisted thereby.

Respectfully submitted,

HUY T. VO

By his Representatives,,
SCHWEGMAN, LUNDBERG, WOESSNER &
KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402

Date ___29 March '06___   By _____
                                          Timothy B. Clise
                                          Reg. No. 40,957